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10/774,374	02/10/2004	Koji Kai	2004_0169A	9530

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EXAMINER	
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2622	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/774,374	KAI ET AL.	
	Examiner	Art Unit	
	Nelson D. Hernández Hernández	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 November 2011*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5)☒ Claim(s) *1-19* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-19* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☒ The drawing(s) filed on *10 February 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

12)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on November 1, 2011 has been entered.

Response to Amendment

2. The Examiner acknowledges the amended claims filed on November 1, 2011. Claims 1, 8 and 12 have been amended.

Response to Arguments

3. Applicant's arguments with respect to claims 1, 8 and 12 have been considered but are moot in view of the new grounds of rejection.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which

said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 2, 7-8, 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Waki et al., EP 1056290 A2 in view of Ichioka, US 2002/0059649 A1.

6. **Regarding claim 1**, **Waki et al.** disclose an integrated circuit (*Fig. 2*) for processing image data (*Col. 8, ¶ 0076, 0079; see also ¶ 0083-0092*), said integrated circuit comprising:

a bus (*Fig. 2: 314*);

a first memory (*Memory Unit 310 and Storage Unit 312 as shown in fig. 2*) connected to said bus (*As shown in fig. 2, the memory unit 310 and the storage unit 312 are connected to bus 314*);

a first processing unit (*CPU 309 as shown in Fig. 2*) operable to access said first memory via said bus (*Waki et al. disclose that when a recorded program needs to be reproduced, the CPU 309 reads the stored information from the storage unit 312 and sends the read digital video information and digital audio information to the video audio decoder (Fig. 2: 306) (Col. 15, ¶ 0091). Note that the CPU 309 access the storage unit 312 though the bus 314 as shown in fig. 2*);

a second processing unit (*The Examiner is interpreting the combination of the Video/Audio Decoder 306 and Demultiplexer 303 shown in fig. 2 as the second processing unit as claimed*) operable to access said first memory via said bus (*Waki et al. disclose that for standard reproduction, the CPU 309 instructs the demultiplexer 303 to directly send the separated digital video information and*

digital audio information to the video/audio decoder 306 and to send the data information to the memory unit 310. Also, when an instruction is made to record a program, the CPU 309 instructs the demultiplexer 303 to send all the separated information to the storage unit 312 (Col. 15, ¶ 0091). Note that in order to send de data information to the memory 310, the demultiplexer access the memory 310 through the bus 314 as shown in fig. 2), and operable to perform at least one of data processing and calculation (*decompression and descrambling of the digital video and audio information that has been compressed according to MPEG (performed by video/audio decoder 306; col. 14, ¶ 0086), and demultiplexing of a transport stream from a tuner (Fig. 2: 302) to separate the transport stream into digital video and audio information (performed by demultiplexer 303; col. 14, ¶ 0085)*), in a larger amount than said first processing unit (*It is noted that the operations performed by the video/audio decoder 306 and demultiplexer 303 (decompression, descrambling and demultiplexing) require larger amount of data processing than the operation performed by the CPU 309 (instructions to control the other processing devices). See col. 14, ¶ 0085-0086; col. 15, ¶ 0089-0092*); and

a second memory (*High-Speed Video Memory Unit 307 as shown in fig. 2*) operable to be accessed by said second processing unit without passing through said bus, such that said second processing unit accesses said second memory without accessing said bus (*Note that the Video/Audio Decoder of the second processing unit (the combination of the Video/Audio Decoder 306 and Demultiplexer 303 as interpreted by the Examiner) access the High-Speed Video*

Memory Unit 307 without accessing the bus 314 as shown in fig. 2. See Col. 14, ¶ 0086),

wherein said second processing unit includes at least one of an image input circuit (*The Demultiplexer of the second processing unit (the combination of the Video/Audio Decoder 306 and Demultiplexer 303 as interpreted by the Examiner) receives as an image input, a transport signal received from an antenna (Fig. 2: 301) (Col. 14, ¶ 0084-0085). Therefore, Waki et al. disclose that the second processing unit includes an image input circuit as claimed*) and an image output circuit (*The Video/Audio Decoder 306 outputs video signals to a TV monitor (Fig. 2: 304) and audio signals to a speaker (Fig. 2: 305) (See col. 14, ¶ 0086). Therefore, Waki et al. disclose that the second processing unit includes an image output circuit as claimed*),

wherein said image input circuit receives output image data from a first component located outside said integrated circuit (*the demultiplexer of the second processing unit (the combination of the Video/Audio Decoder 306 and Demultiplexer 303 as interpreted by the Examiner) receives as an image input, a transport signal received from an antenna (Fig. 2: 301) (Col. 14, ¶ 0084-0085)*), and

wherein said image output circuit generates video signals for outputting to a second component located outside said integrated circuit (*The Video/Audio Decoder 306 decompress the video and audio information and outputs video signals to a TV monitor (Fig. 2: 304) and audio signals to a speaker (Fig. 2: 305) (See col. 14, ¶ 0086)*).

Waki et al. does not explicitly disclose that said second memory is connected only to said second processing unit.

However, **Ichioka** teaches an integrated circuit (*See fig. 4: 11*) for processing image data (*As discussed in ¶ 0060-0073*), said integrated circuit comprising:

a bus (*Fig. 4: 79*);

a first memory (*Ram 82 as shown in fig. 4*) connected to said bus (See fig. 4);

a first processing unit (*Fig. 4: 81*) operable to access said first memory via said bus (*See fig. 4; ¶ 0071*);

a second processing unit (*Fig. 4: 73*) operable to perform at least one of data processing and calculation (*¶ 0062, 0064 and 0066*); and

a second memory (*Fig. 4: 74, ¶ 0064*) operable to be accessed by said second processing unit without passing through said bus, such that said second processing unit accesses said second memory without accessing said bus (*Note that the second memory is directly connected to the decoder 73 so that the decoder 73 access the second memory 74 without passing through said bus 79*),

wherein said second processing unit includes at least one of an image input circuit (*Fig. 4: 84; ¶ 0072*) and an image output circuit (*Fig. 4: 77; ¶ 0064-0065*),

wherein said image input circuit receives output image data from a camera device (*Fig. 4: 92*) connectable to said integrated circuit (*See fig. 4: 11; ¶ 0072*),

wherein said image output circuit generates video signals for outputting to a second component (*display 94 as shown in fig. 4*) located outside said integrated circuit (*¶ 0044, 0048, 0064 and 0068*), and

wherein said second memory (*Fig. 4: 74*) is connected only to said second processing unit (*Note in fig. 4, that the second memory 74 is connected directly to the decoder 73. Note that the RAM 74 is a working memory for said decoder 73. See also ¶ 0064*).

Therefore, taking the combined teaching of Waki et al. in view of Ichioka as a whole, after considering the use of a second memory (*RAM 74*) connected only to a second processing unit (*decoder 73*) as a working memory as taught by Ichioka, it would have been obvious to one of an ordinary skill in the art at the time the invention was made to modify the teaching of Waki to have said second memory connected only to said second processing unit. The motivation to do so would have been to provide an alternative way for the second processor (*decoder 306*) to access the memory (*307*) used to perform its image processing while providing similar results as the second processor would still access the second memory directly without passing through the bus (*Considering that Waki et al. discloses that the memory 307 is used by the decoder for performing a decompression function similar to Ichioka which also teaches performing a decompression function by the decoder 73 using the RAM 74 as a work memory*).

7. **Regarding claim 2**, **Waki et al.** disclose that said image output circuit generates a video signal for outputting to a display device connectable to said integrated circuit, so as to display an image according to the generated video signal (*The Video/Audio Decoder 306 decompress the video and outputs video signals to a connected TV monitor (Fig. 2: 304) (See col. 14, ¶ 0086)*).

Waki et al. do not explicitly disclose that said image input circuit receives the output image data from a camera device connectable to said integrated circuit.

On the other hand, **Ichioka** discloses that said image input circuit (Fig. 4: 84) receives the output image data from a camera device (*Fig. 4: 92*) connectable to said integrated circuit (*See fig. 4: 11; ¶ 0072*).

Therefore, taking the combined teaching of Waki et al. in view of Ichioka as a whole, after acknowledging the concept of receiving image data from a camera device connected to the device 11 in Ichioka, it would have been obvious to one of an ordinary skill in the art at the time the invention was made to modify the teaching of Waki et al. to have said image input circuit receives the output image data from a camera device connectable to said integrated circuit. The motivation to do so would have been to receive additional data from another device increasing the type of sources managed by the integrated circuit for further display.

8. **Regarding claim 7**, **Waki et al.** disclose further comprising a control unit (*IR Data Send/Receive Unit 311 as shown in fig. 2*) operable to control at least

one of said first processing unit and said second processing unit (*Waki et al. disclose that the IR data send/receive unit 311 receives an IR signal that shows a viewer operation from an operating device (203/204 as shown in fig. 1), and sends data showing the viewer operation to the CPU 309. The viewer operation gives an instruction to the receiving device 202, such as to receive and reproduce a program, to receive and record a program, or to reproduce a program that it has recorded*).

9. **Regarding claim 8**, **Waki et al.** disclose an electric device (*Receiving Device 202 as shown in fig. 1*) comprising:

an integrated circuit (*See fig. 2*) for processing image data (*Col. 8, ¶ 0076, 0079; see also ¶ 0083-0092*); and

a converter (*Video/Audio Decoder 306 as shown in fig. 2, which decompresses the video and audio information and outputs video signals to a TV monitor (Fig. 2: 304) and audio signals to a speaker (Fig. 2: 305) (See col. 14, ¶ 0086)*),

wherein said integrated circuit comprises:

a bus (*Fig. 2: 314*);

a first memory (*Memory Unit 310 and Storage Unit 312 as shown in fig. 2*) connected to said bus (*As shown in fig. 2, the memory unit 310 and the storage unit 312 are connected to bus 314*);

a first processing unit (*CPU 309 as shown in Fig. 2*) operable to access said first memory via said bus (*Waki et al. disclose that when a recorded*

program needs to be reproduced, the CPU 309 reads the stored information from the storage unit 312 and sends the read digital video information and digital audio information to the video audio decoder (Fig. 2: 306) (Col. 15, ¶ 0091). Note that the CPU 309 access the storage unit 312 though the bus 314 as shown in fig. 2);

a second processing unit (*The Examiner is interpreting the combination of the Video/Audio Decoder 306 and Demultiplexer 303 shown in fig. 2 as the second processing unit as claimed*) operable to access said first memory via said bus (*Waki et al. disclose that for standard reproduction, the CPU 309 instructs the demultiplexer 303 to directly send the separated digital video information and digital audio information to the video/audio decoder 306 and to send the data information to the memory unit 310. Also, when an instruction is made to record a program, the CPU 309 instructs the demultiplexer 303 to send all the separated information to the storage unit 312 (Col. 15, ¶ 0091). Note that in order to send de data information to the memory 310, the demultiplexer access the memory 310 through the bus 314 as shown in fig. 2*), and operable to perform at least one of data processing and calculation (*decompression and descrambling of the digital video and audio information that has been compressed according to MPEG (performed by video/audio decoder 306; col. 14, ¶ 0086), and demultiplexing of a transport stream from a tuner (Fig. 2: 302) to separate the transport stream into digital video and audio information (performed by demultiplexer 303; col. 14, ¶ 0085)*), in a larger amount than said first processing unit (*It is noted that the operations performed by the video/audio*

decoder 306 and demultiplexer 303 (decompression, descrambling and demultiplexing) require larger amount of data processing than the operation performed by the CPU 309 (instructions to control the other processing devices). See col. 14, ¶ 0085-0086; col. 15, ¶ 0089-0092); and

a second memory (*High-Speed Video Memory Unit 307 as shown in fig. 2*) operable to be accessed by said second processing unit without passing through said bus, such that said second processing unit accesses said second memory without accessing said bus (*Note that the Video/Audio Decoder of the second processing unit (the combination of the Video/Audio Decoder 306 and Demultiplexer 303 as interpreted by the Examiner) access the High-Speed Video Memory Unit 307 without accessing the bus 314 as shown in fig. 2. See Col. 14, ¶ 0086*),

wherein said second processing unit includes at least one of an image input circuit (*The Demultiplexer of the second processing unit (the combination of the Video/Audio Decoder 306 and Demultiplexer 303 as interpreted by the Examiner) receives as an image input, a transport signal received from an antenna (Fig. 2: 301) (Col. 14, ¶ 0084-0085). Therefore, Waki et al. disclose that the second processing unit includes an image input circuit as claimed*) and an image output circuit (*The Video/Audio Decoder 306 outputs video signals to a TV monitor (Fig. 2: 304) and audio signals to a speaker (Fig. 2: 305) (See col. 14, ¶ 0086). Therefore, Waki et al. disclose that the second processing unit includes an image output circuit as claimed*),

wherein said image input circuit receives output image data from a first component located outside said integrated circuit (*the demultiplexer of the second processing unit (the combination of the Video/Audio Decoder 306 and Demultiplexer 303 as interpreted by the Examiner) receives as an image input, a transport signal received from an antenna (Fig. 2: 301) (Col. 14, ¶ 0084-0085)*), and

wherein said image output circuit generates video signals for outputting to a second component located outside said integrated circuit (*The Video/Audio Decoder 306 decompress the video and audio information and outputs video signals to a TV monitor (Fig. 2: 304) and audio signals to a speaker (Fig. 2: 305) (See col. 14, ¶ 0086)*).

Waki et al. does not explicitly disclose that said second memory is connected only to said second processing unit.

However, **Ichioka** teaches an integrated circuit (*See fig. 4: 11*) for processing image data (*As discussed in ¶ 0060-0073*), said integrated circuit comprising:

a bus (*Fig. 4: 79*);

a first memory (*Ram 82 as shown in fig. 4*) connected to said bus (See fig. 4);

a first processing unit (*Fig. 4: 81*) operable to access said first memory via said bus (*See fig. 4; ¶ 0071*);

a second processing unit (*Fig. 4: 73*) operable to perform at least one of data processing and calculation (*¶ 0062, 0064 and 0066*); and

a second memory (*Fig. 4: 74, ¶ 0064*) operable to be accessed by said second processing unit without passing through said bus, such that said second processing unit accesses said second memory without accessing said bus (*Note that the second memory is directly connected to the decoder 73 so that the decoder 73 access the second memory 74 without passing through said bus 79*),

wherein said second processing unit includes at least one of an image input circuit (*Fig. 4: 84; ¶ 0072*) and an image output circuit (*Fig. 4: 77; ¶ 0064-0065*),

wherein said image input circuit receives output image data from a camera device (*Fig. 4: 92*) connectable to said integrated circuit (*See fig. 4: 11; ¶ 0072*),

wherein said image output circuit generates video signals for outputting to a second component (*display 94 as shown in fig. 4*) located outside said integrated circuit (*¶ 0044, 0048, 0064 and 0068*), and

wherein said second memory (*Fig. 4: 74*) is connected only to said second processing unit (*Note in fig. 4, that the second memory 74 is connected directly to the decoder 73. Note that the RAM 74 is a working memory for said decoder 73. See also ¶ 0064*).

Therefore, taking the combined teaching of Waki et al. in view of Ichioka as a whole, after considering the use of a second memory (*RAM 74*) connected only to a second processing unit (*decoder 73*) as a working memory as taught by Ichioka, it would have been obvious to one of an ordinary skill in the art at the time the invention was made to modify the teaching of Waki to have said second memory connected only to said second processing unit. The

motivation to do so would have been to provide an alternative way for the second processor (*decoder 306*) to access the memory (*307*) used to perform its image processing while providing similar results as the second processor would still access the second memory directly without passing through the bus (*Considering that Waki et al. discloses that the memory 307 is used by the decoder for performing a decompression function similar to Ichioka which also teaches performing a decompression function by the decoder 73 using the RAM 74 as a work memory*).

10. **Regarding claim 15**, the Examiner notes that the limitations of claim 15 are written as alternative limitations by reciting "said second processing unit performs at least one of: (i) compressing image data stored in said second memory; (ii) expanding compressed data to image data; (iii) generating image data using a computer graphics operation; and (iv) processing/editing image data, while said first processing unit performs, using said first memory, processing other than the at least of (i), (ii), (iii) and (iv) performed by said second processing unit". **Waki et al.** disclose that said second processing unit performs expanding compressed data to image data (*See col. 14, ¶ 0086*), while said first processing unit performs, using said first memory, processing other than the at least of (i), (ii), (iii) and (iv) performed by said second processing unit (*The first processing unit in Waki et al. performs instructions to control the other processing devices also 309 reads the stored information from the storage unit*

312 and sends the read digital video information and digital audio information to the video audio decoder. See col. 14, ¶ 0085-0086; col. 15, ¶ 0089-0092).

11. **Regarding claim 16**, **Waki et al.** disclose that said image output circuit generates a video signal for outputting to a display device connectable to said integrated circuit, so as to display an image according to the generated video signal (*The Video/Audio Decoder 306 decompress the video and outputs video signals to a connected TV monitor (Fig. 2: 304) (See col. 14, ¶ 0086)*).

Waki et al. do not explicitly disclose that said image input circuit receives the output image data from a camera device connectable to said integrated circuit.

On the other hand, **Ichioka** discloses that said image input circuit (Fig. 4: 84) receives the output image data from a camera device (*Fig. 4: 92*) connectable to said integrated circuit (*See fig. 4: 11; ¶ 0072*).

Therefore, taking the combined teaching of Waki et al. in view of Ichioka as a whole, after acknowledging the concept of receiving image data from a camera device connected to the device 11 in Ichioka, it would have been obvious to one of an ordinary skill in the art at the time the invention was made to modify the teaching of Waki et al. to have said image input circuit receives the output image data from a camera device connectable to said integrated circuit. The motivation to do so would have been to receive additional data from another device increasing the type of sources managed by the integrated circuit for further display.

12. Claims 6, 12 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Waki et al., EP 1056290 A2 in view of Ichioka, US 2002/0059649 A1 and further in view of Ohba, US Patent 6,714,660 B1.

13. **Regarding claim 6**, the combined teaching of Waki et al. in view of Ichioka fails to teach that said second processing unit generates computer graphics image data.

However, **Ohba** teaches an integrated circuit (*See fig. 2*) for processing image data (*Col. 3, lines 6-39*), said integrated circuit comprising:

a bus (*Fig. 2: 34*);

a first memory (*Fig. 2: 32*) connected to said bus (*Note in fig. 2 that the main memory unit 32 is connected to said bus 34*);

a first processing unit (*Fig. 2: 31*) operable to access said first memory via said bus (*Note in fig. 2 that the main CPU 31 access said first memory via said bus. See col. 3, lines 10-15*);

a second processing unit (*The Examiner is interpreting the combination of the rendering engine 41 and the PCRTC circuit 44 as the second processing circuit as claimed*) operable to perform at least one of data processing and calculation (*Col. 3, lines 17-28; col. 5, lines 3-18*), wherein said second processing unit further combine computer graphic with video output from a camera controlled by the CPU 39 (*Fig. 2: 35*) (*See col. 3, lines 16-39; col. 5, line 55 - col. 6, line 15*); and

a second memory (*Fig. 2: 43*) operable to be accessed by said second processing unit without passing through said bus, such that said second

processing unit accesses said second memory without accessing said bus (*Note in fig. 2, that the second memory 43 is directly accessed by the processing unit without passing through said bus 34. See col. 3, lines 17-27*),

wherein said second processing unit includes at least one of an image input circuit (*the second processing unit (the combination of the rendering engine 41 and the PCRTC circuit 44 as interpreted by the Examiner) receives image data from a camera (Fig. 2: 35; see col. 3, lines 29-39; col. 5, lines 35-46; col. 5, line 63 – col. 6, line 15). Therefore, Ohba discloses that the second processing unit includes an image input circuit as claimed*) and an image output circuit (*the second processing unit (the combination of the rendering engine 41 and the PCRTC circuit 44 as interpreted by the Examiner) outputs video signal to a CRT monitor (Fig. 2: 36; see col. 3, lines 29-39). Therefore, Ohba discloses that the second processing unit includes an image output circuit as claimed*),

wherein said image input circuit receives output image data from a camera device (*Fig. 2: 35*) connectable to said integrated circuit (*the second processing unit (the combination of the rendering engine 41 and the PCRTC circuit 44 as interpreted by the Examiner) receives image data from a camera (Fig. 2: 35; see col. 3, lines 29-39; col. 5, lines 35-46; col. 5, line 63 – col. 6, line 15)*),

wherein said image output circuit generates video signals for outputting to a second component (*CRT monitor 36 as shown in fig. 2*) located outside said integrated circuit (*the second processing unit (the combination of the rendering engine 41 and the PCRTC circuit 44 as interpreted by the Examiner) outputs video signal to a CRT monitor (Fig. 2: 36; see col. 3, lines 29-39)*).

Therefore, after considering the teaching of Ohba, which teaches using the second processing unit to create combined image data including computer graphics and video data to modify the second processing unit in Waki et al. and Ichioka to further generate computer graphics image data with the motivation of interactively enhancing the displayed data from the camera with computer graphics so that the user can enjoy the image data including more features as discussed in Ohba (*Col. 1, lines 26-37; col. 5, line 63 – col. 6, line 15*).

14. **Regarding claim 12**, **Waki et al.** disclose an electric device (*Fig. 2*) comprising:

an integrated circuit (*See fig. 2*) for processing image data (*Col. 8, ¶ 0076, 0079; see also ¶ 0083-0092*); and

a converter (*Video/Audio Decoder 306 as shown in fig. 2, which decompresses the video and audio information and outputs video signals to a TV monitor (Fig. 2: 304) and audio signals to a speaker (Fig. 2: 305) (See col. 14, ¶ 0086)*),

wherein said integrated circuit comprises:

a bus (*Fig. 2: 314*);

a first memory (*Memory Unit 310 and Storage Unit 312 as shown in fig. 2*) connected to said bus (*As shown in fig. 2, the memory unit 310 and the storage unit 312 are connected to bus 314*);

a first processing unit (*CPU 309 as shown in Fig. 2*) operable to access said first memory via said bus (*Waki et al. disclose that when a recorded*

program needs to be reproduced, the CPU 309 reads the stored information from the storage unit 312 and sends the read digital video information and digital audio information to the video audio decoder (Fig. 2: 306) (Col. 15, ¶ 0091). Note that the CPU 309 access the storage unit 312 though the bus 314 as shown in fig. 2);

a second processing unit (*The Examiner is interpreting the combination of the Video/Audio Decoder 306 and Demultiplexer 303 shown in fig. 2 as the second processing unit as claimed*) operable to access said first memory via said bus (*Waki et al. disclose that for standard reproduction, the CPU 309 instructs the demultiplexer 303 to directly send the separated digital video information and digital audio information to the video/audio decoder 306 and to send the data information to the memory unit 310. Also, when an instruction is made to record a program, the CPU 309 instructs the demultiplexer 303 to send all the separated information to the storage unit 312 (Col. 15, ¶ 0091). Note that in order to send de data information to the memory 310, the demultiplexer access the memory 310 through the bus 314 as shown in fig. 2*), and operable to perform at least one of data processing and calculation (*decompression and descrambling of the digital video and audio information that has been compressed according to MPEG (performed by video/audio decoder 306; col. 14, ¶ 0086), and demultiplexing of a transport stream from a tuner (Fig. 2: 302) to separate the transport stream into digital video and audio information (performed by demultiplexer 303; col. 14, ¶ 0085)*), in a larger amount than said first processing unit (*It is noted that the operations performed by the video/audio decoder 306*

and demultiplexer 303 (decompression, descrambling and demultiplexing) require larger amount of data processing than the operation performed by the CPU 309 (instructions to control the other processing devices). See col. 14, ¶ 0085-0086; col. 15, ¶ 0089-0092); and

a second memory (*High-Speed Video Memory Unit 307 as shown in fig. 2*) operable to be accessed by said second processing unit without passing through said bus, such that said second processing unit accesses said second memory without accessing said bus (*Note that the Video/Audio Decoder of the second processing unit (the combination of the Video/Audio Decoder 306 and Demultiplexer 303 as interpreted by the Examiner) access the High-Speed Video Memory Unit 307 without accessing the bus 314 as shown in fig. 2. See Col. 14, ¶ 0086*),

wherein said second processing unit includes at least one of an image input circuit (*The Demultiplexer of the second processing unit (the combination of the Video/Audio Decoder 306 and Demultiplexer 303 as interpreted by the Examiner) receives as an image input, a transport signal received from an antenna (Fig. 2: 301) (Col. 14, ¶ 0084-0085). Therefore, Waki et al. disclose that the second processing unit includes an image input circuit as claimed*) and an image output circuit (*The Video/Audio Decoder 306 outputs video signals to a TV monitor (Fig. 2: 304) and audio signals to a speaker (Fig. 2: 305) (See col. 14, ¶ 0086). Therefore, Waki et al. disclose that the second processing unit includes an image output circuit as claimed*),

wherein said image input circuit receives output image data from a first component located outside said integrated circuit (*the demultiplexer of the second processing unit (the combination of the Video/Audio Decoder 306 and Demultiplexer 303 as interpreted by the Examiner) receives as an image input, a transport signal received from an antenna (Fig. 2: 301) (Col. 14, ¶ 0084-0085)*), and

wherein said image output circuit generates video signals for outputting to a second component located outside said integrated circuit (*The Video/Audio Decoder 306 decompress the video and audio information and outputs video signals to a TV monitor (Fig. 2: 304) and audio signals to a speaker (Fig. 2: 305) (See col. 14, ¶ 0086)*).

Waki et al. do not explicitly disclose a camera, a microphone and a converter.

However, **Ichioka** discloses an electric device (Fig. 4) comprising:

a camera (Fig. 4: 92);

an integrated circuit for processing image data (Fig. 4: 11); and

wherein said integrated circuit comprises:

a bus (*Fig. 4: 79*);

a first memory (*Ram 82 as shown in fig. 4*) connected to said bus (See fig. 4);

a first processing unit (*Fig. 4: 81*) operable to access said first memory via said bus (*See fig. 4; ¶ 0071*);

a second processing unit (*Fig. 4: 73*) operable to perform at least one of data processing and calculation (*¶ 0062, 0064 and 0066*); and

a second memory (*Fig. 4: 74, ¶ 0064*) operable to be accessed by said second processing unit without passing through said bus, such that said second processing unit accesses said second memory without accessing said bus (*Note that the second memory is directly connected to the decoder 73 so that the decoder 73 access the second memory 74 without passing through said bus 79*),

wherein said second processing unit includes at least one of an image input circuit (*Fig. 4: 84; ¶ 0072*), and an image output circuit (*Fig. 4: 77; ¶ 0064-0065*),

wherein said image input circuit receives output image data from a first component (*Fig. 4: 92*) located outside said integrated circuit (*See fig. 4: 11; ¶ 0072*),

wherein said image output circuit generates video signals for outputting to a second component (*display 94 as shown in fig. 4*) located outside said integrated circuit (*¶ 0044, 0048, 0064 and 0068*), and

wherein said second memory (*Fig. 4: 74*) is connected only to said second processing unit (*Note in fig. 4, that the second memory 74 is connected directly to the decoder 73. Note that the RAM 74 is a working memory for said decoder 73. See also ¶ 0064*).

Therefore, taking the combined teaching of Waki et al. in view of Ichioka as a whole, after acknowledging the concept of receiving image data from a camera device connected to the device 11 in Ichioka, it would have been obvious

to one of an ordinary skill in the art at the time the invention was made to modify the teaching of Waki et al. to have said image input circuit receives the output image data from a camera device connectable to said integrated circuit. The motivation to do so would have been to receive additional data from another device increasing the type of sources managed by the integrated circuit for further display.

The combined teaching of Waki et al. in view of Ichioka fails to teach a microphone and a converter.

However, **Ohba** discloses an electric device comprising:

a camera (*Fig. 2: 35*);

a microphone (*Fig. 2: 38*);

an integrated circuit (*See fig. 2*) for processing image data (*Col. 3, lines 6-39*); and

a converter operable to input analog audio signals from said microphone to convert the analog audio signals into digital audio signals (*Ohba discloses the use of an audio processing chip (Fig. 2: 37) that received audio data input by the microphone 38 to transmit the audio data through the internet to another image processing device (Col. 3, lines 40-48). This teaches the use of a converter as claimed*), and operable to output the digital audio signals to said first processing unit (*The main CPU 31 (first processing unit as claimed) controls the audio processing chip and causes audio data from the microphone to be transmitted from communication unit through internet to a server. See col. 7, lines 4-7*);

wherein said integrated circuit comprises:

a bus (*Fig. 2: 34*);

a first memory (*Fig. 2: 32*) connected to said bus (*Note that memory 32 is connected to said bus 34 as shown in fig. 2*);

a first processing unit (*Fig. 2: 31*) operable to access said first memory via said bus (*Note in fig. 2 that the main CPU 31 access said first memory via said bus. See col. 3, lines 10-15*);

a second processing unit (*The Examiner is interpreting the combination of the rendering engine 41 and the PCRTC circuit 44 as the second processing circuit as claimed*), and operable to perform at least one of data processing and calculation (*Col. 3, lines 17-28; col. 5, lines 3-18*), in a larger amount than said first processing unit (*The rendering engine 41 and PCRTC 44 perform drawing processing at high speed to an image memory 43, while the PCRTC control in real time the position, size and resolution of the image data input from the camera 35 to send the modified video signal to a CRT monitor 36 (Col. 3, lines 16-39) while the first processing unit 31 controls the operation of the processing unit 33 (which includes the second processing unit), generate processing commands to said second processing unit (Col. 3, lines 10-15) and perform feature extraction on the received video to be latter combined to the computer graphics in the rendering engine and the PCRTC (Col. 4, lines 20-28, lines 46-53; col. 5, lines 3-18). It is noted that in combination, the rendering engine 41 and the PCRTC circuit 44 (which is being interpreted as the second processing unit as claimed), perform larger amount of processing than said first processing unit*); and

a second memory (*Fig. 2: 43*) operable to be accessed by said second processing unit without passing through said bus, such that said second processing unit accesses said second memory without accessing said bus (*Note in fig. 2, that the second memory 43 is directly accessed by the processing unit without passing through said bus 34. See col. 3, lines 17-27*),

wherein said second processing unit includes at least one of an image input circuit (*the second processing unit (the combination of the rendering engine 41 and the PCRTC circuit 44 as interpreted by the Examiner) receives image data from a camera (Fig. 2: 35; see col. 3, lines 29-39; col. 5, lines 35-46; col. 5, line 63 – col. 6, line 15). Therefore, Ohba discloses that the second processing unit includes an image input circuit as claimed*), and an image output circuit (*the second processing unit (the combination of the rendering engine 41 and the PCRTC circuit 44 as interpreted by the Examiner) outputs video signal to a CRT monitor (Fig. 2: 36; see col. 3, lines 29-39). Therefore, Ohba discloses that the second processing unit includes an image output circuit as claimed*),

wherein said image input circuit receives output image data from a first component (*Camera 35 as shown in fig. 2*) located outside said integrated circuit (*the second processing unit (the combination of the rendering engine 41 and the PCRTC circuit 44 as interpreted by the Examiner) receives image data from a camera (Fig. 2: 35; see col. 3, lines 29-39; col. 5, lines 35-46; col. 5, line 63 – col. 6, line 15)*), and

wherein said image output circuit generates video signals for outputting to a second component (*CRT monitor 36 as shown in fig. 2*) located

outside said integrated circuit (*the second processing unit (the combination of the rendering engine 41 and the PCRTC circuit 44 as interpreted by the Examiner) outputs video signal to a CRT monitor (Fig. 2: 36; see col. 3, lines 29-39)*).

wherein said second memory (*Fig. 2: 43*) is connected to said second processing unit (*through memory interface 42 as shown in fig. 2*).

Therefore, taking the combined teaching of Waki et al. in view of Ichioka and further in view of Ohba as a whole, after considering the concept of having a microphone to receive audio data and a converter to process said received audio data for further transmission to a remote device as taught by Ohba, it would have been obvious to one of an ordinary skill in the art at the time the invention was made to modify the teaching of Waki et al. and Ichioka to further include a microphone and a converter. The motivation to do so would have been to allow the integrated circuit to receive audio signals for further processing and transmission to an external device as suggested by Ohba (*Col. 3, lines 40-48 and col. 7, lines 4-7*).

15. **Regarding claim 18**, the combined teaching of Waki et al. in view of Ichioka and further in view of Ohba further teaches that said image input circuit receives the output image data from said camera (*Ohba discloses that the PCRTC 44 receives the image data from the camera 35*), which is connectable to said integrated circuit (*Note that the camera is connectable to said integrated circuit as shown in figs. 2, 6 and 12*) (*See col. 3, lines 29-39; col. 5, lines 35-46; col. 5, line 63 – col. 6, line 15)*), and wherein said image output circuit generates

a video signal for outputting to a display device (*CRT monitor as shown in fig. 2*) connectable to said integrated circuit block (*Note that the monitor is connected to said integrated circuit as shown in figs. 2, 6 and 12*), so as to display an image according to the generated video signal (*the second processing unit (the combination of the rendering engine 41 and the PCRTC circuit 44 as interpreted by the Examiner) outputs video signal to a CRT monitor (See col. 3, lines 29-39)*). Thus, it would have been obvious to one of an ordinary skill in the art at the time the invention was made to modify the teaching of Waki et al. and Ichioka to further have said image input circuit receives the output image data from said camera, which is connectable to said integrated circuit, and wherein said image output circuit generates a video signal for outputting to a display device connectable to said integrated circuit block, so as to display an image according to the generated video signal with the motivation of increase the capabilities of the integrated device by allowing reception of additional data from another device increasing the type of sources managed by the integrated circuit for further display.

16. Claims 3, 4, 17, 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Waki et al., EP 1056290 A2 in view of Ichioka, US 2002/0059649 A1 and further in view of Kawakami et al., 2002/0012522 A1.

17. **Regarding claim 3**, **Waki et al.** disclose that the second processing unit expands compressed video signals (*col. 14, ¶ 0086*). However, the teaching of Waki et al. in view of Ichioka fails to teach that said first processing unit expands

compressed audio signals, and wherein said second processing unit stores reference image data into said second memory, the reference image data being generated when the compressed video signals are expanded.

However, **Kawakami et al.** teaches a camera circuit (*See fig. 4*) comprising a first memory (*Fig. 4: 32*); a sound compression Encoder/Decoder (*Fig. 4: 37, the Examiner is interpreting the sound compression Encoder/Decoder as a first processing unit*) operable to access said first memory (*Page 8, ¶ 0150*), said compression Encoder/Decoder, operable to compress and decompress the sound from the video (*Page 8, ¶ 0150, 0158, 0165*); an MPEG2 video signal Processing (*Fig. 4: 33, the Examiner is interpreting the MPEG2 video signal Processing as a second processing unit*) operable to access said first memory (*Page 8, ¶ 0156*), said MPEG2 video signal Processing operable to compress and decompress the video signal (*Page 7, ¶ 0144-0148; page 8, ¶ 0156-0157*), and operable to perform at least one of data processing and calculation in a larger amount than said first processing unit (*It is noted that the video processing in the MPEG2 video signal Processing requires calculation in a larger amount than the sound compression Encoder/Decoder*), wherein the MPEG2 video signal processing expands compressed video signals, and wherein said second processing unit stores reference image data into said second memory (*It is noted that the second memory is a dedicated memory for the compression/expansion processing and the video signal is temporally stored in the second memory (Page 7, ¶ 0144), the reference image data being generated when the compressed video signals are expanded (It is also noted that the MPEG2*

compression/decompression uses P-frames (Predictive frames) when performing compression/decompression that would later be used for either compressing or expanding the video signals, depending on the application (either reading or writing video data). Therefore, Kawakami et al. further said second processing unit stores reference image data into said second memory, the reference image data being generated when the compressed video signals are expanded as claimed); and a second memory (*Fig. 4: 34*) operable to be directly accessed by said second processing (*Page 8, ¶ 0156*).

Therefore, taking the combined teaching of Waki et al. in view of Ichioka and further in view of Kawakami et al. as a whole, it would have been obvious to one of an ordinary skill in the art at the time the invention was made to apply the concept of using a dedicated processing unit for video compression and decompression having a dedicated memory for processing the video signals and a processing unit of compression and decompression of audio signals as taught in Kawakami et al. to modify the teaching of Waki et al. and Ohba to have the first processing unit expanding compressed audio signals as an alternative instead of using the second processing unit in Waki et al. while obtaining predictable results (outputting audio signals which have been processed from a different device without changing the main operation of the integrated circuit), and to have the second processing unit storing reference image data into said second memory, the reference image data being generated when the compressed video signals are expanded with the motivation of allowing quick decompression of the image signals by using the reference data stored in the

dedicated memory as can be appreciated from the Kawakami et al. teaching (Page 8, ¶ 0144) to improve the processing units in Waki et al. by allowing recording and playback moving picture data and edit recorded moving picture data.

18. **Regarding claim 4**, the combined teaching of Waki et al. in view of Ichioka fails to teach that said first processing unit compresses audio signals, wherein said second processing unit compresses video signals, and wherein said second processing unit stores reference image data into said second memory, the reference image data being generated when the compressed video signals are expanded.

However, **Kawakami et al.** teaches a camera circuit (*See fig. 4*) comprising a first memory (*Fig. 4: 32*); a sound compression Encoder/Decoder (*Fig. 4: 37, the Examiner is interpreting the sound compression Encoder/Decoder as a first processing unit*) operable to access said first memory (*Page 8, ¶ 0150*), said compression Encoder/Decoder, operable to compress and decompress the sound from the video (*Page 8, ¶ 0150, 0158, 0165*); an MPEG2 video signal Processing (*Fig. 4: 33, the Examiner is interpreting the MPEG2 video signal Processing as a second processing unit*) operable to access said first memory (*Page 8, ¶ 0156*), said MPEG2 video signal Processing operable to compress and decompress the video signal (*Page 7, ¶ 0144-0148; page 8, ¶ 0156-0157*), and operable to perform at least one of data processing and calculation in a larger amount than said first processing unit (*It is noted that the video processing*

in the MPEG2 video signal processing requires calculation in a larger amount than the sound compression Encoder/Decoder), wherein the MPEG2 video signal Processing expands compressed video signals, and wherein said second processing unit stores reference image data into said second memory (It is noted that the second memory is a dedicated memory for the compression/expansion processing and the video signal is temporally stored in the second memory (*Page 7, ¶ 0144*), the reference image data being generated when the compressed video signals are expanded (*It is also noted that the MPEG2 compression/decompression uses P-frames (Predictive frames) when performing compression/decompression that would later be used for either compressing or expanding the video signals, depending on the application (either reading or writing video data). Therefore, Kawakami et al. further teaches that the second processing unit expands compressed video signals, and wherein said second processing unit stores reference image data into said second memory, the reference image data being generated when the compressed video signals are expanded as claimed*); and a second memory (*Fig. 4: 34*) operable to be directly accessed by said second processing (*Page 8, ¶ 0156*).

Therefore, taking the combined teaching of Waki et al. in view of Ichioka and further in view of Kawakami et al. as a whole, it would have been obvious to one of an ordinary skill in the art at the time the invention was made to apply the concept of using a dedicated processing unit for video compression and decompression having a dedicated memory for processing the video signals and a processing unit of compression and decompression of audio signals as taught

in Kawakami et al. to modify the teaching of Waki et al. and Ichioka to have the first processing unit compressing audio signals which improve the storage space in memory; to have said second processing unit storing reference image data into said second memory, the reference image data being generated when the compressed video signals are expanded with the motivation of allowing quick decompression of the image signals by using the reference data stored in the dedicated memory as can be appreciated from the Kawakami et al. teaching (*Page 8, ¶ 0144*) to improve the processing units in Waki et al. by allowing recording and playback moving picture data and edit recorded moving picture data.

19. **Regarding claim 17**, **Waki et al.** disclose that the second processing unit expands compressed video signals to generate video signals (*col. 14, ¶ 0086*) and that the converter convert the audio signals expanded by the second processing unit into analog audio signals (*See col. 14, ¶ 0086. The Examiner understands the decompressed digital audio signal by the video/audio decoder 306 needs to further be converted into analog signal before being output to the speaker*) but the combined teaching of Waki et al. in view of Ichioka fails to teach that said first processing unit expands compressed audio signals, that said second processing unit stores reference image data into said second memory, the reference image data being generated when the compressed video signals are expanded, and that said conversion of the audio signals into analog audio signals is performed on audio signals expanded by said first processing unit

(being different in that Waki et al. teach that the conversion is made to signals expanded in the second processing unit).

However, **Kawakami et al.** teaches a camera circuit (*See fig. 4*) comprising a first memory (*Fig. 4: 32*); a sound compression Encoder/Decoder (*Fig. 4: 37, the Examiner is interpreting the sound compression Encoder/Decoder as a first processing unit*) operable to access said first memory (*Page 8, ¶ 0150*), said compression Encoder/Decoder, operable to compress and decompress the sound from the video (*Page 8, ¶ 0150, 0158, 0165*), wherein the output of said sound compression Encoder/Decoder is sent to a converter (*Fig. 4: 65*) to convert the expanded audio signals into analog audio signals to be output to a speaker (*Fig. 4: 205*) (*Page 8, ¶ 0165-0166*); an MPEG2 video signal Processing (*Fig. 4: 33, the Examiner is interpreting the MPEG2 video signal Processing as a second processing unit*) operable to access said first memory (*Page 8, ¶ 0156*), said MPEG2 video signal Processing operable to compress and decompress the video signal (*Page 7, ¶ 0144-0148; page 8, ¶ 0156-0157*), and operable to perform at least one of data processing and calculation in a larger amount than said first processing unit (*It is noted that the video processing in the MPEG2 video signal Processing requires calculation in a larger amount than the sound compression Encoder/Decoder*), wherein the MPEG2 video signal processing expands compressed video signals, and wherein said second processing unit stores reference image data into said second memory (*It is noted that the second memory is a dedicated memory for the compression/expansion processing and the video signal is temporally stored in the second memory (Page 7, ¶ 0144), the*

reference image data being generated when the compressed video signals are expanded (It is also noted that the MPEG2 compression/decompression uses P-frames (Predictive frames) when performing compression/decompression that would later be used for either compressing or expanding the video signals, depending on the application (either reading or writing video data). Therefore, Kawakami et al. further said second processing unit stores reference image data into said second memory, the reference image data being generated when the compressed video signals are expanded as claimed); and a second memory (*Fig. 4: 34*) operable to be directly accessed by said second processing (*Page 8, ¶ 0156*).

Therefore, taking the combined teaching of Waki et al. in view of Ichioka and further in view of Kawakami et al. as a whole, it would have been obvious to one of an ordinary skill in the art at the time the invention was made to apply the concept of using a dedicated processing unit for video compression and decompression having a dedicated memory for processing the video signals and a processing unit of compression and decompression of audio signals that sends the expanded audio signals to a converter to convert the signals into analog signals to be sent to a speaker for reproduction as taught in Kawakami et al. to modify the teaching of Waki et al. to have the first processing unit expanding compressed audio signals to be converted into analog by the converter as an alternative instead of using the second processing unit in Waki et al. and Ichioka while obtaining predictable results (outputting audio signals which have been processed from a different device without changing the main operation of the

integrated circuit), and to have the second processing unit storing reference image data into said second memory, the reference image data being generated when the compressed video signals are expanded with the motivation of allowing quick decompression of the image signals by using the reference data stored in the dedicated memory as can be appreciated from the Kawakami et al. teaching (*Page 8, ¶ 0144*) to improve the processing units in Waki et al. by allowing recording and playback moving picture data and edit recorded moving picture data.

20. **Regarding claim 9**, **Waki et al.** disclose that said integrated circuit further comprises a control unit (*IR Data Send/Receive Unit 311 as shown in fig. 2*) operable to control at least one of said first processing unit and said second processing unit (*Waki et al. disclose that the IR data send/receive unit 311 receives an IR signal that shows a viewer operation from an operating device (203/204 as shown in fig. 1), and sends data showing the viewer operation to the CPU 309. The viewer operation gives an instruction to the receiving device 202, such as to receive and reproduce a program, to receive and record a program, or to reproduce a program that it has recorded*).

21. **Regarding claim 10**, **Waki et al.** disclose a display device (*TV monitor 304 as shown in fig. 2*) operable to input the video signals generated by said second processing unit to display an image (*See col. 14, ¶ 0086*); and a playback device

(*Speaker 305 as shown in fig. 2*) operable to reproduce sounds according to the analog analogue audio signals converted by said converter (*See col. 14, ¶ 0086. The Examiner understands the decompressed digital audio signal by the video/audio decoder 306 needs to further be converted into analog signal before being output to the speaker*).

22. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Waki et al., EP 1056290 A2 and Ichioka, US 2002/0059649 A1 in view of Kawakami et al., 2002/0012522 A1 and further in view of Ohba, US Patent 6,714,660 B1.

23. **Regarding claim 11**, the combined teaching of Waki et al. in view of Ichioka and further in view of Kawakami et al. fails to teach that said second processing unit generates computer graphics image data.

However, **Ohba** teaches an integrated circuit (*See fig. 2*) for processing image data (*Col. 3, lines 6-39*), said integrated circuit comprising:

a bus (*Fig. 2: 34*);

a first memory (*Fig. 2: 32*) connected to said bus (*Note in fig. 2 that the main memory unit 32 is connected to said bus 34*);

a first processing unit (*Fig. 2: 31*) operable to access said first memory via said bus (*Note in fig. 2 that the main CPU 31 access said first memory via said bus. See col. 3, lines 10-15*);

a second processing unit (*The Examiner is interpreting the combination of the rendering engine 41 and the PCRTC circuit 44 as the second processing*

circuit as claimed) operable to perform at least one of data processing and calculation (*Col. 3, lines 17-28; col. 5, lines 3-18*), wherein said second processing unit further combine computer graphic with video output from a camera controlled by the CPU 39 (*Fig. 2: 35*) (*See col. 3, lines 16-39; col. 5, line 55 - col. 6, line 15*); and

a second memory (*Fig. 2: 43*) operable to be accessed by said second processing unit without passing through said bus, such that said second processing unit accesses said second memory without accessing said bus (*Note in fig. 2, that the second memory 43 is directly accessed by the processing unit without passing through said bus 34. See col. 3, lines 17-27*),

wherein said second processing unit includes at least one of an image input circuit (*the second processing unit (the combination of the rendering engine 41 and the PCRTC circuit 44 as interpreted by the Examiner) receives image data from a camera (Fig. 2: 35; see col. 3, lines 29-39; col. 5, lines 35-46; col. 5, line 63 – col. 6, line 15). Therefore, Ohba discloses that the second processing unit includes an image input circuit as claimed*) and an image output circuit (*the second processing unit (the combination of the rendering engine 41 and the PCRTC circuit 44 as interpreted by the Examiner) outputs video signal to a CRT monitor (Fig. 2: 36; see col. 3, lines 29-39). Therefore, Ohba discloses that the second processing unit includes an image output circuit as claimed*),

wherein said image input circuit receives output image data from a camera device (*Fig. 2: 35*) connectable to said integrated circuit (*the second processing unit (the combination of the rendering engine 41 and the PCRTC circuit 44 as*

interpreted by the Examiner) receives image data from a camera (Fig. 2: 35; see col. 3, lines 29-39; col. 5, lines 35-46; col. 5, line 63 – col. 6, line 15)),

wherein said image output circuit generates video signals for outputting to a second component (*CRT monitor 36 as shown in fig. 2*) located outside said integrated circuit (*the second processing unit (the combination of the rendering engine 41 and the PCRTC circuit 44 as interpreted by the Examiner) outputs video signal to a CRT monitor (Fig. 2: 36; see col. 3, lines 29-39)*).

Therefore, after considering the teaching of Ohba, which teaches using the second processing unit to create combined image data including computer graphics and video data to modify the second processing unit to further generate computer graphics image data with the motivation of interactively enhancing the displayed data from the camera with computer graphics so that the user can enjoy the image data including more features as discussed in Ohba (*Col. 1, lines 26-37; col. 5, line 63 – col. 6, line 15*).

24. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Waki et al., EP 1056290 A2 in view of Ichioka, US 2002/0059649 A1 and further in view of Applicants Admitted Prior Art (thereinafter referred as AAPA).

25. **Regarding claim 5**, the combined teaching of Waki et al. in view of Ichioka fails to teach that said first processing unit performs at least one of de-multiplexing audio signals and video signals from a bit stream and multiplexing audio signals and video signals into a bit stream.

However, **AAPA** teaches an integrated circuit comprising: a bus (*Fig. 2: 2*); a first memory connected to said bus (*Fig. 2: 3*); a first processing unit (Fig. 2: 6) operable to access said first memory via said bus (*See fig. 2*) and operable to perform at least one of de-multiplexing audio signals and video signals from a bit stream and multiplexing audio signals and video signals into a bit stream (*Page 2, ¶ 0012-0015*); a second processing unit (*Fig. 2: 4*) operable to access said first memory via said bus (*See fig. 2*), and operable to perform at least one of data processing and calculation in a larger amount than said first processing unit (*Video processing unit 4 perform image processing which requires more capacity that the audio processed by audio processor 5*); and a second memory (*buffer 7 as shown in fig. 2*) operable to be accessed by said second processing unit without passing through said bus (*Note that the buffer 7 is operable to be directly accessed by the second processing unit as shown in fig. 2*).

Therefore, taking the combined teaching of Waki et al. in view of Ichioka and further in view of AAPA as a whole, it would have been obvious to one of an ordinary skill in the art at the time the invention was made to apply the concept of having a multiplex/de-multiplex circuit for de-multiplexing audio signals and video signals from a bit stream or multiplexing audio signals and video signals into a bit stream to have the first processing unit performing at least one of de-multiplexing audio signals and video signals from a bit stream and multiplexing audio signals and video signals into a bit stream as an alternative to the second processing unit as it is done in Waki et al. with the motivation of providing a multiprocessor

configuration in which different processors perform specific operation as taught in AAPA.

26. Claims 19, 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Waki et al., EP 1056290 A2 and Ichioka, US 2002/0059649 A1 in view of Ohba, US Patent 6,714,660 B1 and further in view of Kawakami et al., 2002/0012522 A1.

27. **Regarding claim 19**, the combined teaching of Waki et al. in view of Ichioka and further in view of Ohba further teaches discloses that said converter (*Ohba, fig. 2: 37*) is operable to input analog audio signals from said microphone to convert the analog audio signals into digital audio signals (*Ohba discloses that the audio processing receives audio data input by the microphone 38 to transmit the audio data through the internet to another image processing device (Col. 3, lines 40-48). This teaches that the converter converts the analog audio signals into digital audio signals since in order to transmit the audio signals, said signals need to be converted to digital format to be transmitted through the internet*), and operable to output the digital audio signals to said first processing unit (*The main CPU 31 (first processing unit as claimed) controls the audio processing chip and causes audio data from the microphone to be transmitted from communication unit through internet to a server. See col. 7, lines 4-7*) and Waki et al. teaches that the second processing unit expands compressed video signals to generate video signals (*col. 14, ¶ 0086*) and that the converter convert the audio signals expanded by the second processing unit into analog audio signals (*See col. 14, ¶*

0086. The Examiner understands the decompressed digital audio signal by the video/audio decoder 306 needs to further be converted into analog signal before being output to the speaker).

However, the combined teaching of Waki et al. in view of Ichioka and further in view of Waki et al. fails to teach that said first processing unit compresses audio signals, that said second processing unit inputs video signals from said camera to compress the video signals, that said second processing unit stores reference image data into said second memory, the reference image data being generated when the compressed video signals are expanded.

However, **Kawakami et al.** teaches a camera circuit (*See fig. 4*) comprising a first memory (*Fig. 4: 32*); a sound compression Encoder/Decoder (*Fig. 4: 37, the Examiner is interpreting the sound compression Encoder/Decoder as a first processing unit*) operable to access said first memory (*Page 8, ¶ 0150*), said compression Encoder/Decoder, operable to compress and decompress the sound from the video (*Page 8, ¶ 0150, 0158, 0165*); an MPEG2 video signal Processing (*Fig. 4: 33, the Examiner is interpreting the MPEG2 video signal Processing as a second processing unit*) operable to access said first memory (*Page 8, ¶ 0156*), said MPEG2 video signal Processing operable to compress and decompress the video signal (*Page 7, ¶ 0144-0148; page 8, ¶ 0156-0157*), and operable to perform at least one of data processing and calculation in a larger amount than said first processing unit (*It is noted that the video processing in the MPEG2 video signal processing requires calculation in a larger amount than the sound compression Encoder/Decoder*), wherein the MPEG2 video

signal Processing expands compressed video signals, and wherein said second processing unit stores reference image data into said second memory (It is noted that the second memory is a dedicated memory for the compression/expansion processing and the video signal is temporally stored in the second memory (*Page 7, ¶ 0144*), the reference image data being generated when the compressed video signals are expanded (*It is also noted that the MPEG2 compression/decompression uses P-frames (Predictive frames) when performing compression/decompression that would later be used for either compressing or expanding the video signals, depending on the application (either reading or writing video data). Therefore, Kawakami et al. further teaches that the second processing unit expands compressed video signals, and wherein said second processing unit stores reference image data into said second memory, the reference image data being generated when the compressed video signals are expanded as claimed*); and a second memory (*Fig. 4: 34*) operable to be directly accessed by said second processing (*Page 8, ¶ 0156*).

Therefore, taking the combined teaching of Waki et al. and Ichioka in view of Ohba and further in view of Kawakami et al. as a whole, it would have been obvious to one of an ordinary skill in the art at the time the invention was made to apply the concept of using a dedicated processing unit for video compression and decompression having a dedicated memory for processing the video signals and a processing unit of compression and decompression of audio signals as taught in Kawakami et al. to modify the teaching of Waki et al., Ichioka and Ohba to have the first processing unit compressing audio signals which improve the

storage space in memory; also to have said second processing unit storing reference image data into said second memory, the reference image data being generated when the compressed video signals are expanded with the motivation of allowing quick decompression of the image signals by using the reference data stored in the dedicated memory as can be appreciated from the Kawakami et al. teaching (*Page 8, ¶ 0144*) to improve the processing units in Waki et al. by allowing recording and playback moving picture data and edit recorded moving picture data.

28. **Regarding claim 13**, the combined teaching of Waki et al. and Ichioka in view of Ohba and further in view of Kawakami et al. further teaches that the second processing unit generates computer graphics image data (*In Ohba, the second processing unit combines computer graphic with video output from a camera controlled by the CPU 39 (Fig. 2: 35) (See col. 3, lines 16-39; col. 5, line 55 - col. 6, line 15). This teaches that the second processing unit generates computer graphics image data as claimed*). Thus, it would have been obvious to one of an ordinary skill in the art at the time the invention was made to modify the second processing unit to further generate computer graphics image data with the motivation of interactively enhancing the displayed data from the camera with computer graphics so that the user can enjoy the image data including more features as discussed in Ohba (*Col. 1, lines 26-37; col. 5, line 63 – col. 6, line 15*).

29. **Regarding claim 14**, the combined teaching of Waki et al. and Ichioka in view of Ohba and further in view of Kawakami et al. further teaches that said integrated circuit further comprises a control unit (*In Waki, fig. 2: 311 (Col. 15, ¶ 0089); In Ohba, Input Unit 30 as shown in fig. 2*) operable to control at least one of said first processing unit and said second processing unit (See Waki et al., *col. 15, ¶ 0089; in Ohba, the user operates the input unit 30 and the CPU 31 operates in accordance to the inputs made by the user. See Col. 6, line 16 – col. 7, line 3*).

Contact

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